ALPHA & OMEGA SEMICONDUCTOR

AOL1424

N-Channel Enhancement Mode Field Effect Transistor

General Description

The AOL1424 uses advanced trench technology to provide excellent $R_{DS(ON)}$, low gate charge and operation with gate voltages as low as 4.5V,while retaining a 20V $V_{GS(MAX)}$ rating. It is ESD protected.This device is suitable for use as a load switch.

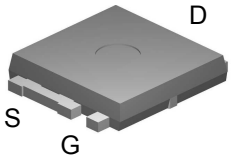
-RoHS Compliant
-Halogen and Antimony Free Green Device*

Features

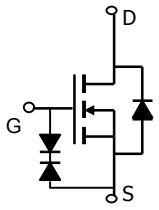
V_{DS} (V) = 30V
I_D = 70A (V_{GS} = 10V)
$R_{DS(ON)}$ < 5.4mΩ (V_{GS} = 10V)
$R_{DS(ON)}$ < 8mΩ (V_{GS} = 4.5V)

ESD Protected
UIS Tested
Rg,Ciss,Coss,Crss Tested

Ultra SO-8™ Top View



Bottom tab connected to drain



Absolute Maximum Ratings T_A=25°C unless otherwise noted

Parameter		Symbol	Maximum	Units
Drain-Source Voltage		V_{DS}	30	V
Gate-Source Voltage		V_{GS}	±20	V
Continuous Drain Current [B]	T_C=25°C	I_D	70	A
	T_C=100°C		50	
Pulsed Drain Current [C]		I_{DM}	120	
Continuous Drain Current [A]	T_A=25°C	I_{DSM}	15	A
	T_A=70°C		12	
Avalanche Current [H]		I_{AR}	30	A
Repetitive avalanche energy L=0.3mH [H]		E_{AR}	135	mJ
Power Dissipation [B]	T_C=25°C	P_D	50	W
	T_C=100°C		25	
Power Dissipation [A]	T_A=25°C	P_{DSM}	2.2	W
	T_A=70°C		1.5	
Junction and Storage Temperature Range		T_J, T_{STG}	-55 to 175	°C

Thermal Characteristics

Parameter		Symbol	Typ	Max	Units
Maximum Junction-to-Ambient [A]	t ≤ 10s	$R_{\theta JA}$	20	24	°C/W
Maximum Junction-to-Ambient [A]	Steady-State		45	55	°C/W
Maximum Junction-to-Case [D]	Steady-State	$R_{\theta JC}$	2.5	3.0	°C/W

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV_{DSS}	Drain-Source Breakdown Voltage	I_D=250µA, V_{GS}=0V	30			V
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS}=30V, V_{GS}=0V			1	µA
		T_J=55°C			5	
I_{GSS}	Gate-Body leakage current	V_{DS}=0V, V_{GS}= ±16V			10	µA
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS}=V_{GS} I_D=250µA	1.4	1.8	2.5	V
$I_{D(ON)}$	On state drain current	V_{GS}=10V, V_{DS}=5V	120			A
$R_{DS(ON)}$	Static Drain-Source On-Resistance	V_{GS}=10V, I_D=20A		4.5	5.4	mΩ
		T_J=125°C		6.3	7.6	
		V_{GS}=4.5V, I_D=20A		6.5	8.0	mΩ
g_{FS}	Forward Transconductance	V_{DS}=5V, I_D=20A		67		S
V_{SD}	Diode Forward Voltage	I_S=1A,V_{GS}=0V		0.7	1.0	V
I_S	Maximum Body-Diode Continuous Current				70	A
DYNAMIC PARAMETERS						
C_{iss}	Input Capacitance	V_{GS}=0V, V_{DS}=15V, f=1MHz		1803	2170	pF
C_{oss}	Output Capacitance			387		pF
C_{rss}	Reverse Transfer Capacitance			238		pF
R_g	Gate resistance	V_{GS}=0V, V_{DS}=0V, f=1MHz		1.3	2	Ω
SWITCHING PARAMETERS						
Q_g(10V)	Total Gate Charge	V_{GS}=10V, V_{DS}=15V, I_D=20A		36	48	nC
Q_g(4.5V)	Total Gate Charge			19		nC
Q_{gs}	Gate Source Charge			3.9		nC
Q_{gd}	Gate Drain Charge			8.7		nC
$t_{D(on)}$	Turn-On DelayTime	V_{GS}=10V, V_{DS}=15V, R_L=0.75Ω, R_{GEN}=3Ω		7.6		ns
t_r	Turn-On Rise Time			6.4		ns
$t_{D(off)}$	Turn-Off DelayTime			27		ns
t_f	Turn-Off Fall Time			8.5		ns
t_{rr}	Body Diode Reverse Recovery Time	I_F=20A, dI/dt=100A/µs		27	33	ns
Q_{rr}	Body Diode Reverse Recovery Charge	I_F=20A, dI/dt=100A/µs		17		nC

A: The value of $R_{\theta JA}$ is measured with the device in a still air environment with T_A =25°C. The power dissipation P_{DSM} and current rating I_{DSM} are based on $T_{J(MAX)}$=150°C, using steady state junction-to-ambient thermal resistance.

B. The power dissipation P_D is based on $T_{J(MAX)}$=175°C, using junction-to-case thermal resistance, and is more useful in setting the upper dissipation limit for cases where additional heatsinking is used.

C: Repetitive rating, pulse width limited by junction temperature $T_{J(MAX)}$=175°C.

D. The $R_{\theta JA}$ is the sum of the thermal impedence from junction to case $R_{\theta JC}$ and case to ambient.

E. The static characteristics in Figures 1 to 6 are obtained using <300µs pulses, duty cycle 0.5% max.

F. These curves are based on the junction-to-case thermal impedence which is measured with the device mounted to a large heatsink, assuming a maximum junction temperature of $T_{J(MAX)}$=175°C.

G. These tests are performed with the device mounted on 1 in 2 FR-4 board with 2oz. Copper, in a still air environment with T_A=25°C. The SOA curve provides a single pulse rating.

H. EAR and IAR ratings are based on low frequency and duty cycles such that Tj(start)=25C for each pulse.

* This device is guaranteed green after date code 8P11 (June 1st 2008)

Rev5: Jul 2008

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

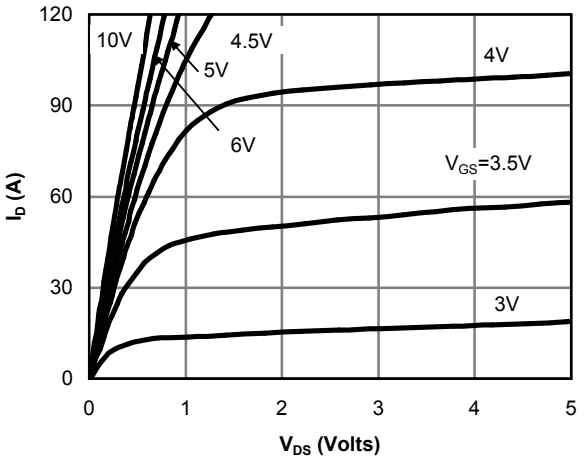


Figure 1: On-Region Characteristics

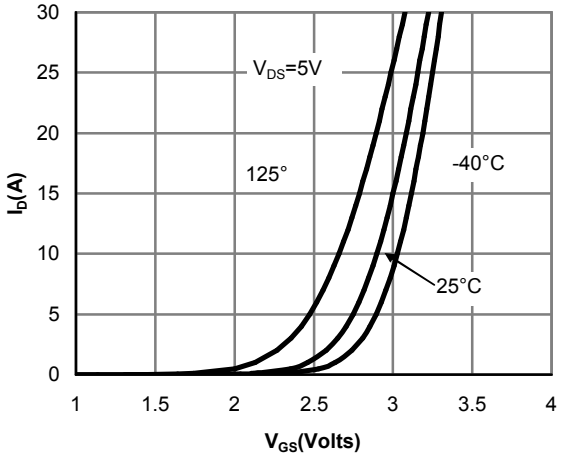


Figure 2: Transfer Characteristics

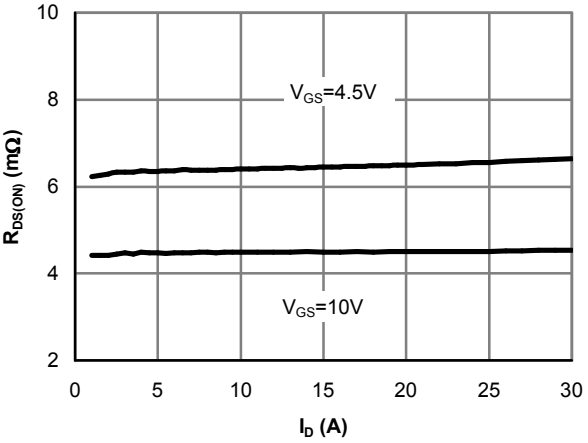


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

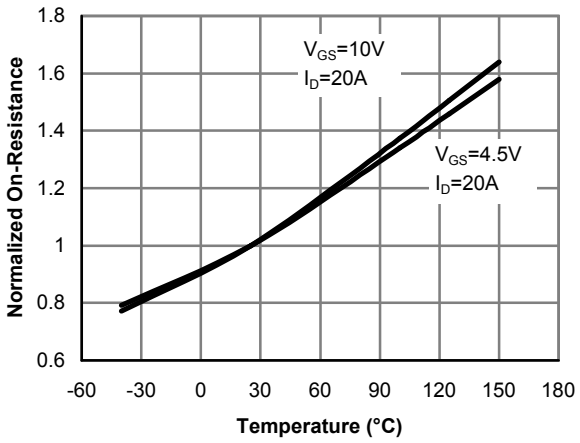


Figure 4: On-Resistance vs. Junction Temperature

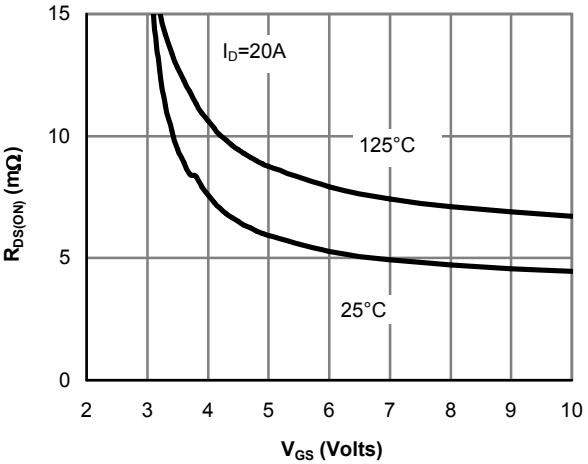


Figure 5: On-Resistance vs. Gate-Source Voltage

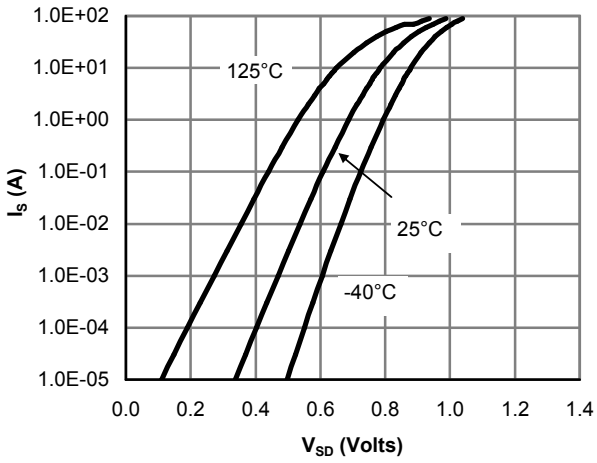


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

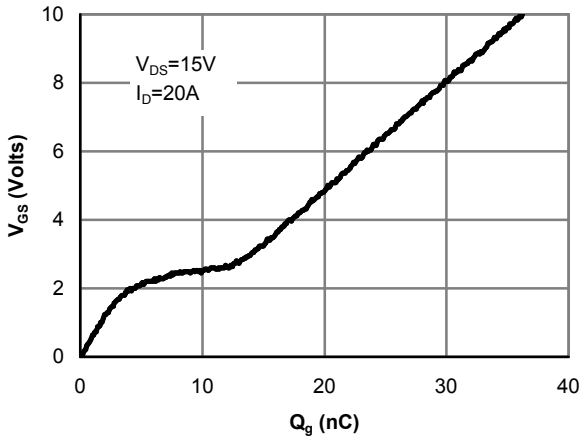


Figure 7: Gate-Charge Characteristics

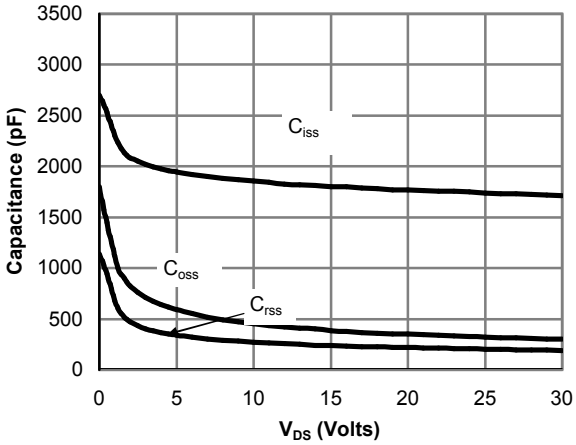


Figure 8: Capacitance Characteristics

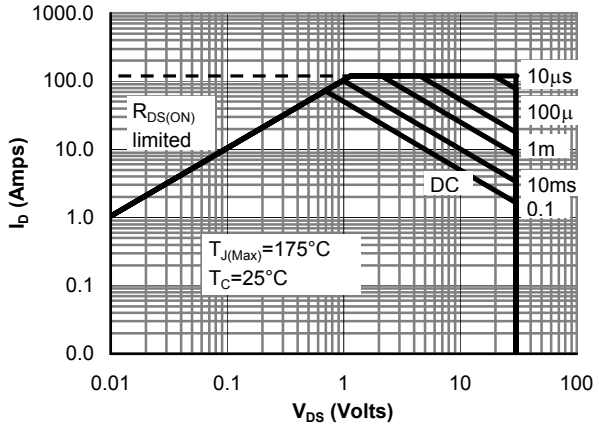


Figure 9: Maximum Forward Biased Safe Operating Area (Note F)

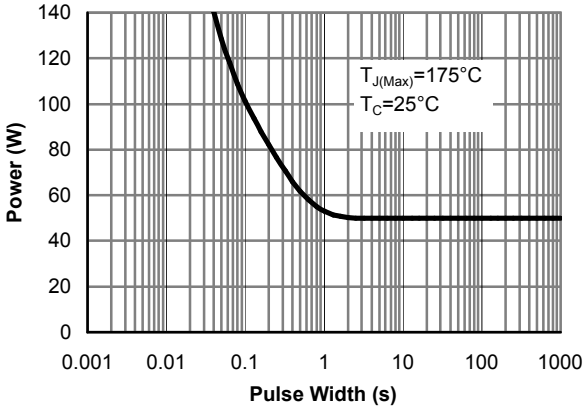


Figure 10: Single Pulse Power Rating Junction-to-Case (Note F)

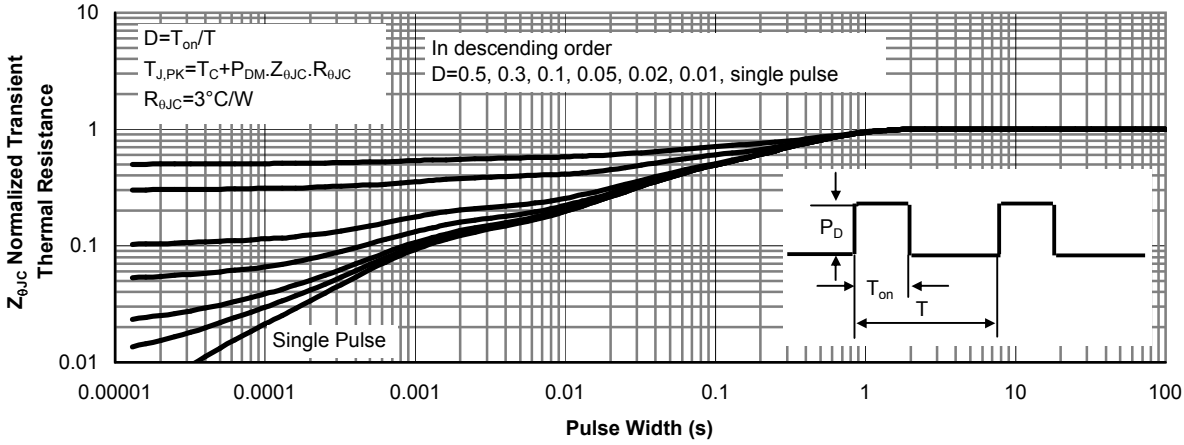


Figure 11: Normalized Maximum Transient Thermal Impedance (Note F)

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

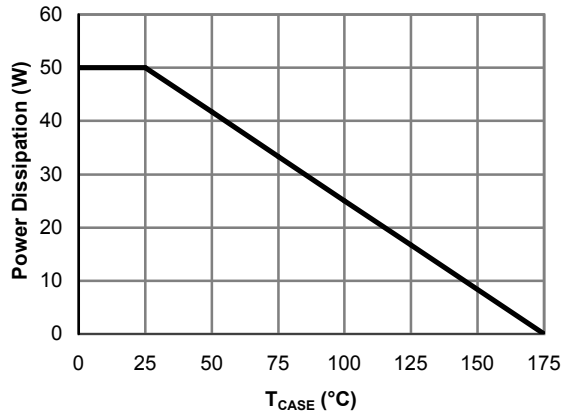


Figure 12: Power De-rating (Note B)

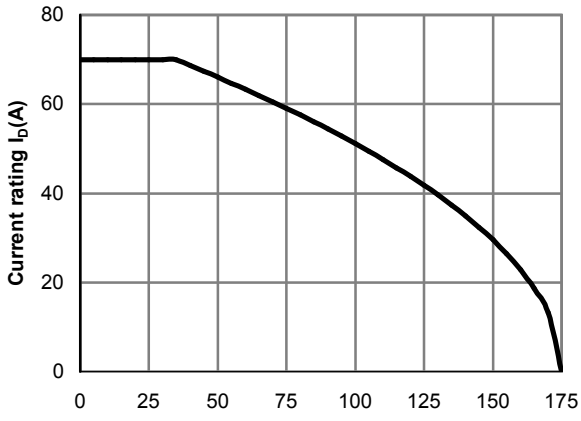


Figure 13: Current De-rating (Note B)

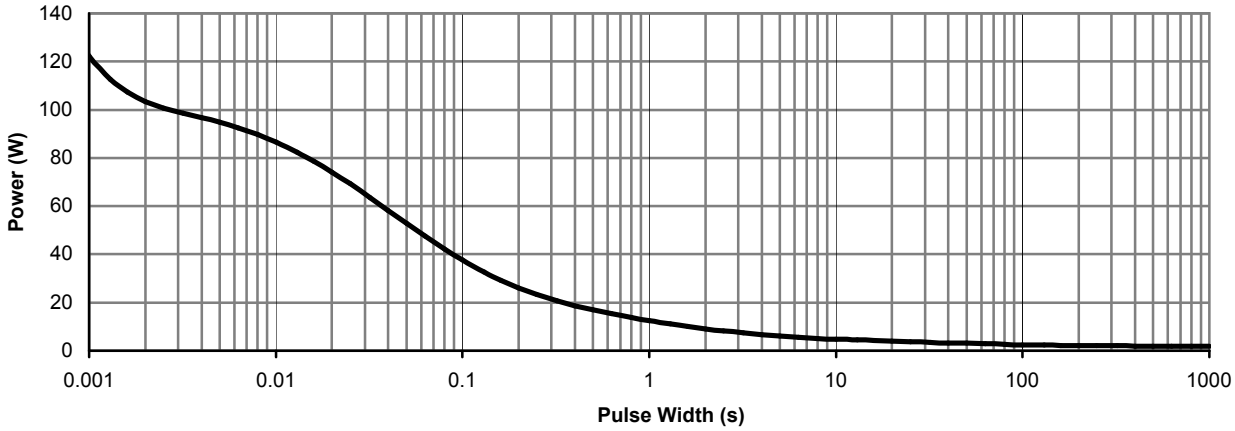


Figure 14: Single Pulse Power Rating Junction-to-Ambient (Note G)

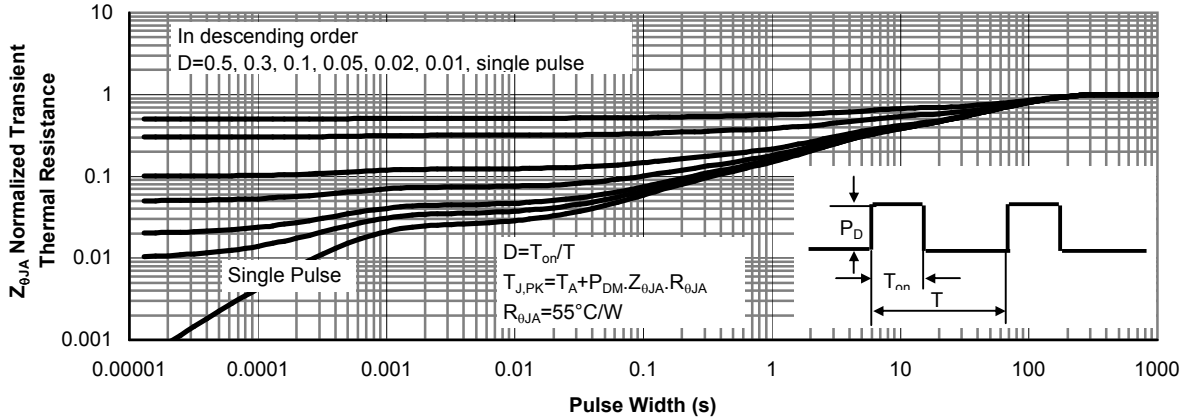
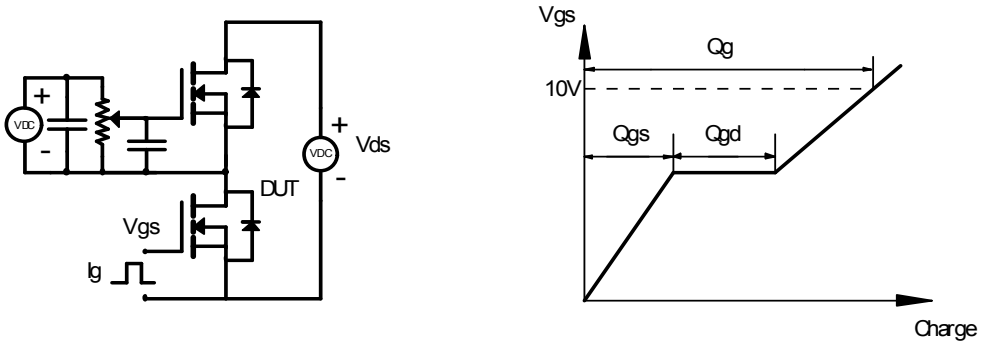
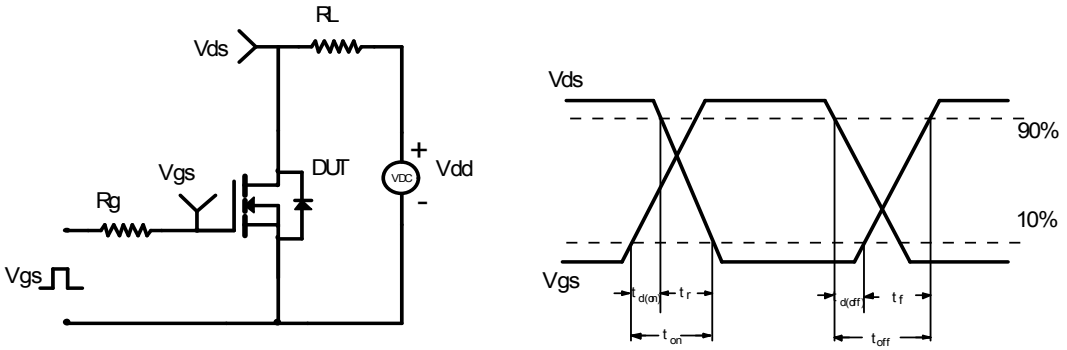


Figure 15: Normalized Maximum Transient Thermal Impedance (Note G)

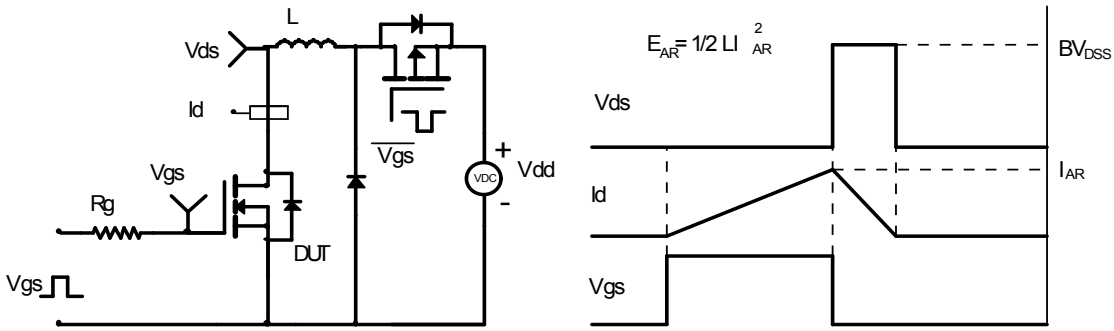
Gate Charge Test Circuit & Waveform



Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms